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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,830	02/11/2002	Richard V. Folea JR.		4629

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/073,830	FOLEA, RICHARD V.
	Examiner	Art Unit
	Cynthia Britt	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) 11 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 and 12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-12 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 8/11/02 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 3.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-12 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on May 1, 2002 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on February 11, 2002. These drawings are acceptable.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 12, drawn to monitoring and controlling target devices in a boundary scan chain, classified in class 714, subclass 727.

II. Claim 11, drawn to determining a sequence of state machine transitions in a TAP controller, classified in class 714, subclass 724.

The inventions are distinct, each from the other because of the following reasons:

Inventions in Group I and Group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II

has separate utility such as can be used in testing of a system or device without the type of user interface and specifics required of Group I. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Richard Folea Jr. on July 8th 2004, a provisional election was made with traverse to prosecute the invention of Group I, claims 1-10 and 12. Affirmation of this election must be made by applicant in replying to this Office action. Claim 11 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "easy-to-use intuitive " in claim 1 is a relative term, which renders the claim indefinite. The term " easy-to-use intuitive " is not defined by the claim, the

specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The term "preparing predetermined test vectors" in claim 3 is a relative term which renders the claim indefinite. The term "preparing" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The term " preparing predetermined test executives" in claim 4 is a relative term which renders the claim indefinite. The term "preparing" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

These phrases are particularly questionable in light of the abstract of the present specification, which states in lines 1 and 2 “does not require the use of test vectors or test executives”, and in line 9 “bypassing the need for test vectors”. Since these items are indicated as not required, it is also unclear to the examiner what would be required to “prepare” the test vectors and test executives.

The term "familiar to the user" in claim 9 is a relative term which renders the claim indefinite. The term " familiar to the user " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the

invention. It is unclear how one of ordinary sill in the art would know what would be familiar to an end user.

As per claim 7, the phrase "graphical representation of various forms of light emitting diodes" is unclear.

Claims 2-10 are dependent on the independent claim 1 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered relative to the prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,279,123 Mulrooney in view of "*JTAG Visualizer Makes Boundary*

Scan Visible Powerful Tool at DFT Assessment and Repair f PCB's" JTAG Technologies Press information release date November 6, 2001.

As per claims 1 and 12, Mulrooney substantially teaches the claimed method of using a host computer monitors the real-time operation of a target device having a scan chain by identifying devices connected to the scan chain, downloading from the host computer to the target device, target programs associated with the identified devices; synchronously running all of the target programs; and transmitting results data, compiled as a result of running the target programs, in real-time to the host computer without interrupting the operation of the target device (column 2 lines 38-50, figure 2). Not explicitly disclosed is the user interaction with the boundary scan elements.

However, in an analogous art, JTAG Technologies disclose a device in which " full graphical interpretation of boundary scan operations" can be graphically displayed with results and user accessibility (page 1 paragraphs 2 and 3). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the full graphical interpretation of boundary scan operations of JTAG Technologies with the method of Mulrooney. This would have been obvious to a person having ordinary skill in the art at the time this invention was made as suggested by Mulrooney (column 4 lines 40-50) in order for the user to more easily understand how a test is progressing.

As per claim 2, JTAG Technologies teach the capability of varying the graphics and colors of the displayed devices (page 1, paragraph 2).

As per claims 3 and 4, in boundary scan testing, the test vectors and test executives would be inherent in this type of testing, whether provided by a file containing these or by a test pattern generator etc. (See above 35 U.S.C. 112, second paragraph rejections of these claims above, also Mulrooney column 3 lines 53-62).

As per claim 5, Mulrooney teaches updating test status of the running tests (column 4 lines 34-39).

As per claims 6 and 7, Mulrooney teaches a GUI which the user can see a displayed indication of current testing processes (column 3 line 36-52).

As per claims 8 and 9, Mulrooney teaches that the command line parameters may be input from the configuration file or can be directly input from the keyboard of the host computer using the host control panel GUI, if the host user wishes to modify the diagnostics specified by the configuration file. (Column 4 lines 46-50 FIG. 2)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,629,282 Sugamori et al.

This patent teaches a semiconductor test system with a graphic user interface (GUI) to function as an interface between the test system and a user. Operations of the test system, creation of test programs, and execution of the test programs are conducted through the work station.

U.S. Patent No. 6,389,565 Ryan et al.

This patent teaches a graphical user interface for displaying boundary scan test data, and method for producing the same, is presented. The user interface display allows a user to view boundary scan test data from a boundary scan testing device in a format suited for debugging. Serial data received from the testing device is organized into a parallel format to display predicted versus actual data values on a per node basis, to show how a node is passing or failing. In a preferred embodiment, the user views the frame cell number in the boundary scan chain, the device cell number within a device at that point of the chain, the device name, the pin of the device associated with the cell, the node associated with the pin, the predicted value for the cell, the actual value for the cell as if differs from the predicted value if it differs, and the cell numbers for drivers that match predicted and actual data.

"*PATRIOT-A Boundary-Scan Test and Diagnosis System*" by Wang et al. Thirty-Seventh IEEE Computer Society International Conference Compcon Spring '92, Digest of Papers 24-28 Feb. 1992 pages 436 - 439 Inspec Accession Number: 4315153

This paper teaches a boundary-scan test and diagnosis system (PATRIOT) for detecting and locating defective chips and interconnects on printed-circuit boards is presented. These printed-circuit boards must be designed with boundary-scan chips conforming to the IEEE 1149.1 Standard. The PATRIOT system consists of interconnect test generation software, protocol interface firmware, X-window user

interface, and a hardware test controller. It can be linked to any workstation or PC computer, which has a SCSI-bus interface. PATRIOT uses the hardware test controller to coordinate data transfer between the computer and the printed-circuit boards. Up to four boards can be tested and diagnosed simultaneously.

"*A Structured Graphical Tool for Analyzing Boundary Scan Violations*" by Cogswell et al. International Test Conference, 2002 Proceedings 7-10 Oct. 2002, pages 755 - 762 Inspec Accession Number: 7528844

This paper teaches that the boundary scan test methodology is becoming an increasingly important approach for testing chips, modules and boards. Commercial boundary scan verification tools are now available which provide a system of checks not only for IEEE 1149.1 but other methodologies such as IBM Boundary Scan. A key factor in the effectiveness of boundary scan verification systems is found in the accuracy and flexibility of companion analysis tools used to correlate the violated boundary scan rule with the subject logic structure causing the violation. This paper presents the design and deployment of a graphical system for pinpointing sources of boundary scan rules violations. The paper begins with a cursory review of boundary scan methodologies including IEEE 1149.1 and IBM Boundary Scan. This is followed by a brief presentation of the boundary scan verification process used in IBM's Test Bench tool. The body of the paper is focused on boundary scan verification rules and the associated message analysis. The paper concludes with future plans under consideration to improve both the reach and usability of graphical message analysis for boundary scan verification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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